What is claimed is:

1. An apparatus comprising:

a first transistor having a current I_{ON} when ON;

a second transistor having a current I_{OFF} when OFF; and

a circuit to body bias the first and second transistors so that when the first and second transistors are at thermal equilibrium with a temperature, the ratio of I_{ON} to I_{OFF} is independent of temperature for a range of the temperature values.

2. The apparatus as set forth in claim 1, the apparatus comprising at least one transistor, wherein the circuit body biases the at least one transistor.

3. The apparatus as set forth in claim 1, wherein the first transistor is a nFET and the second transistor is a nFET.

4. The apparatus as set forth in claim 1, wherein the first transistor is a pFET and the second transistor is a pFET.

5. The apparatus as set forth in claim 1, wherein the first transistor has a first channel length, and the second transistor has a second channel length equal to the first channel length.

6. The apparatus as set forth in claim 5, wherein the first transistor has a first channel width, and the second transistor has a second channel width equal to the first channel width.

7. The apparatus as set forth in claim 1, the first transistor comprising a body terminal and the second transistor comprising a body terminal, the circuit comprising:

a node;

a first current mirror connected to the first transistor and the node;

a second current mirror connected to the second transistor and the node; and

an amplifier comprising an input port connected to the node and an output port connected to the body terminals of the first and second transistors.

8. A circuit comprising:

a node;

a first transistor comprising a body terminal, the first transistor to provide a current I_{ON} when ON;

a first current mirror coupled to the first transistor to source to the node a first current proportional to I_{ON};

a second transistor comprising a body terminal, the second transistor to provide a current I_{OFF} when OFF;

a second current mirror coupled to the first transistor to sink from the node a second current proportional to I_{OFF}, and

an amplifier coupled to the node and to provide a bias voltage to the body terminals of the first and second transistors so that under steady state the first and second currents are equal to each other.

9. The circuit as set forth in claim 8, wherein

the first transistor is a nFET comprising a gate, and a drain connected to its gate;

the second transistor is a nFET comprising a gate, and a source connected to its gate.

10. The circuit as set forth in claim 8, wherein

the first transistor is a pFET comprising a gate, and a drain connected to its gate;

the second transistor is a pFET comprising a gate, and a source connected to its gate.

11. The circuit as set forth in claim 8, wherein the first transistor has a first channel length, and the second transistor has a second channel length equal to the first channel length.

12. The apparatus as set forth in claim 11, wherein the first transistor has a first channel width, and the second transistor has a second channel width equal to the first channel width.

13. A circuit comprising:

a node;

a first transistor comprising a body terminal, the first transistor to provide a current I_{ON} when ON;

a first current mirror coupled to the first transistor to sink from the node a first current proportional to I_{ON};

a second transistor comprising a body terminal, the second transistor to provide a current I_{OFF} when OFF;

a second current mirror coupled to the first transistor to source to the node a second current proportional to I_{OFF}, and

an amplifier coupled to the node and to provide a bias voltage to the body terminals of the first and second transistors so that under steady state the first and second currents are equal to each other.

14. The circuit as set forth in claim 13, wherein

the first transistor is a nFET comprising a gate, and a drain connected to its gate;

the second transistor is a nFET comprising a gate, and a source connected to its gate.

15. The circuit as set forth in claim 13, wherein

the first transistor is a pFET comprising a gate, and a drain connected to its gate;

the second transistor is a pFET comprising a gate, and a source connected to its gate.

16. The circuit as set forth in claim 13, wherein the first transistor has a first channel length, and the second transistor has a second channel length equal to the first channel length.

17. The apparatus as set forth in claim 16, wherein the first transistor has a first channel width, and the second transistor has a second channel width equal to the first channel width.

18. A circuit comprising:

a node;

a first transistor comprising a body terminal, and having a current I_{ON} when ON;

a first current mirror connected to the first transistor to mirror I_{ON} with a first gain to the node;

a second transistor comprising a body terminal, and having a current I_{OFF} when OFF;

a second current mirror connected to the second transistor to mirror I_{OFF} with a second gain from the node; and

an amplifier comprising an input port connected to the node and comprising an output port connected to the body terminals of the first and second transistors.

19. The circuit as set forth in claim 18, wherein the first transistor is a nFET and the second transistor is a nFET, wherein the amplifier has an input-output relationship $V_{out} = \alpha V_{node} + V_0$, where is α is a positive scalar and V_0 is an offset voltage.

20. The circuit as set forth in claim 18, wherein the first transistor is a pFET and the second transistor is a pFET, wherein the amplifier has an input-output relationship $V_{out} = \alpha V_{node} + V_0$, where is α is a negative scalar and V_0 is an offset voltage.

21. The circuit as set forth in claim 18, wherein the first transistor has a first channel length, and the second transistor has a second channel length equal to the first channel length.

22. The apparatus as set forth in claim 21, wherein the first transistor has a first channel width, and the second transistor has a second channel width equal to the first channel width.

23. A circuit comprising:

a node;

a first transistor comprising a body terminal, and having a current I_{ON} when ON;

a first current mirror connected to the first transistor to mirror I_{ON} with a first gain from the node;

a second transistor comprising a body terminal, and having a current I_{OFF} when OFF;

a second current mirror connected to the second transistor to mirror I_{OFF} with a second gain to the node; and

an amplifier comprising an input port connected to the node and comprising an output port connected to the body terminals of the first and second transistors.

24. The circuit as set forth in claim 23, wherein the first transistor is a nFET and the second transistor is a nFET, wherein the amplifier has an input-output relationship $V_{out} = \alpha V_{node} + V_0$, where is α is a negative scalar and V_0 is an offset voltage.

25. The circuit as set forth in claim 23, wherein the first transistor is a pFET and the second transistor is a pFET, wherein the amplifier has an input-output relationship $V_{out} = \alpha V_{node} + V_0$, where is α is a positive scalar and V_0 is an offset voltage.

26. The circuit as set forth in claim 23, wherein the first transistor has a first channel length, and the second transistor has a second channel length equal to the first channel length.

27. The apparatus as set forth in claim 26, wherein the first transistor has a first channel width, and the second transistor has a second channel width equal to the first channel width.

28. A system comprising a die and a cache not on the die, the die comprising:

a first transistor having a current I_{ON} when ON;

a second transistor having a current I_{OFF} when OFF; and

a circuit to body bias the first and second transistors so that when the first and second transistors are at thermal equilibrium with a temperature, the ratio of I_{ON} to I_{OFF} is independent of temperature for a range of the temperature values.

29. The system as set forth in claim 28, the die comprising at least one transistor, wherein the circuit body biases the at least one transistor.

30. The system as set forth in claim 28, the first transistor comprising a body terminal and the second transistor comprising a body terminal, the circuit comprising:

a node;

a first current mirror connected to the first transistor and the node;

a second current mirror connected to the second transistor and the node; and

an amplifier comprising an input port connected to the node and an output port connected to the body terminals of the first and second transistors.